REMARKS/ARGUMENTS

This Response is submitted in reply to the Office Action dated February 2, 2006, and within the three month period extending to May 2, 2006. Claims 1-20 remain pending following entry of this Response.

Allowable Subject Matter

The Applicants acknowledge the Office's indication that claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Rejections under 35 U.S.C. 102

Claim 1 was rejected under 35 U.S.C. 102(e) as being anticipated by Herz et al. ("Herz" hereafter) (U.S. Patent No. 6,965,956). This rejection is traversed.

Herz teaches a disk array controller that is capable of detecting and controlling both SATA and SAS disk drives. Herz (1:55-58) teaches that once the type of a given disk drive has been determined, the disk array controller uses a corresponding protocol (ATA or SCSI) to communicate with that disk drive. Herz (2:50-53) also teaches that the disk array controller includes a respective controller (40) for each disk drive port available on the disk array controller. Each controller (40) for the various disk drive ports of the disk array controller is disclosed by Herz (2:53-55) as including logic for implementing both the SATA protocol and the SAS protocol. Herz (4:38-42) teaches that each controller (40) enters into a mode in which it uses either a SATA or SAS protocol, as appropriate, to communicate with the disk drive to which it is connected. Herz (4:19-24) further teaches that a microcontroller (56) within the disk array controller sends disk

drive commands in a SATA format to a controller (40) that controls a SATA drive. Similarly, Herz (4:19-24) teaches that the microcontroller (56) sends disk drive commands in a SAS format to a controller (40) that controls a SAS drive.

Based on the foregoing, it should be appreciated that the disk array controller of Herz teaches duplication of disk drive control circuitry to accommodate operation in accordance with both the SAS and SATA protocols. Herz does not teach that the disk array controller includes logic defined to operate in accordance with a data format that is neutral to both the SAS and SATA protocols. Specifically, with regard to claim 1, Herz does not teach wired endian logic configured to interface a wired endian format with each of a big endian format of a SAS protocol device and a little endian format of a SATA protocol device. Simply stated, in contrast to having wired endian logic, Herz includes both SAS logic and SATA logic that will be utilized depending on whether a particular disk drive is of SAS format or of SATA format, respectively. Additionally, Herz does not teach the disk array controller as including internal circuitry configured to operate in accordance with the wired endian format.

The Office is respectfully reminded that a claim is anticipated under 35 U.S.C. 102 only when each and every feature of the claim is taught by a single reference. Therefore, based on the foregoing, the Applicants submit that Herz fails to teach each and every feature of claim 1. Thus, the Applicants kindly request the Office to withdraw the outstanding rejection of claim 1.

Rejections under 35 U.S.C. 103

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune et al. ("Brune" hereafter) (U.S. Patent No. 6,622,187 B1) in view of Crawford et al. ("Crawford" hereafter) (U.S. Patent No. 5,948,099). This rejection is traversed.

Brune (6:15-18) teaches a multiplexing device (24) defined to perform byte reordering from big endian type to little endian type, wherein the multiplexing device (24) is controlled by a little endian flag (23) in a status register (22). The multiplexing device (24) is implemented within an application data processing unit (30) that is connected to receive packetized communications from an IEEE1394 interface. The IEEE1394 data link integrated circuit is of big endian type. Therefore, if the application data processing unit (30) is of little endian type, it is necessary to reorder the bytes transmitted through the IEEE1394 interface to the application data processing unit (30) from big endian type to little endian type. In the case where the application data processing unit (30) is of little endian type, the little endian flag (23) is set to "1", to indicate that the big endian-to-little endian conversion needs to be performed by the multiplexing device (24). In the case where the application data processing unit (30) is of big endian type, the little endian flag (23) is set to "0", to indicate that the big endian-to-little endian conversion does not need to be performed by the multiplexing device (24).

Based on the foregoing, it should be appreciated that Brune teaches conversion of transmitted multi-byte data words from big endian format to little endian format, when the receiving device is defined to operate in accordance with little endian format. Although Brune teaches conversion from big endian format to little endian format, Brune is completely silent with regard to conversion from big endian format to wired endian format. Furthermore, Brune is equally silent with regard to conversion from little endian format to wired endian format. Additionally, Brune does not include any teaching of a wired endian format. Brune's teachings are simply associated with big endian format and little endian format, and the conversion therebetween.

Based on the foregoing, and in contrast to the Office's assertions, the Applicants do find any teaching of the following features of claim 11 in Brune:

- identifying a sequence of bytes to be transmitted as one of a control sequence of bytes and a data sequence of bytes, the sequence of bytes to be transmitted being maintained in a wired endian format;
- converting the sequence of bytes having been identified as the data sequence of bytes from the wired endian format to a native format, wherein the native format is associated with a device to which the sequence of bytes is to be transmitted;
- transmitting the sequence of bytes in accordance with the wired endian format.

The Office has indicated that Brune does not disclose converting the data sequence of bytes from the native format to the wired endian format. The Applicants agree with this indication by the Office. The Office has, however, asserted that Crawford teaches converting the data sequence of bytes from the native format to the wired endian format. The Applicants respectfully disagree with this assertion by the Office.

Crawford teaches a barrel shifter for performing a byte swap operation to convert a multi-byte data word from big endian format to little endian format, vice-versa. The Office has asserted the Crawford (2:56-60) teaches the feature of claim 11 for "converting the data sequence of bytes from the native format to the wired endian format." Crawford (2:56-60) states the following:

"The presently described byte swap instruction allows the programmer to convert data from a big-endian memory format to a little-endian data format, and back again, without incurring the performance penalties associated with past microprocessors."

The Applicants submit that Crawford, particularly (2:56-60), is completely silent with regard to a wired endian format. Moreover, the Applicants submit that Crawford,

particularly (2:56-60), is completely silent with regard to converting a data sequence of bytes from a native format to a wired endian format.

In view of the foregoing and in contrast to the Office's assertions, the Applicants submit that the combination of Brune and Crawford fails to teach each and every feature of claim 11. To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. Therefore, the Applicants submit that the combination of Brune and Crawford fails to render claim 11 prima facie obvious under 35 U.S.C. 103. Thus, the Applicants kindly request the Office to withdraw the outstanding rejection of claim 11.

In point number 16 of the outstanding Office Action, the Office has indicated that claims 12-15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Crawford, and further in view of Beigel et al. ("Beigel" hereafter) (U.S. Patent No. 6,472,975 B1). However, rather than discussing the rejections of claims 12-15 the Office discusses the rejection of claim 16 with respect to the combination of Brune, Crawford, and Beigel. Therefore, the Applicants assume that identification of claims 12-15 in point number 16 of the outstanding Office Action is a mistake. Thus, the Applicant considers that claim 16 was rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Crawford, and further in view of Beigel. This rejection of claim 16 is traversed.

With regard to claim 16, the Office has asserted that Crawford teaches an operation for converting a sequence of bytes from a native format to a wired endian format. As discussed above with regard to claim 11, Crawford, particularly (2:56-60), is completely silent with regard to a wired endian format. Moreover, Crawford, particularly (2:56-60), is completely silent with regard to converting a sequence of bytes from a native format to a wired endian format.

As previously mentioned, a claim can only be rendered prima facie obvious when the combined cited art of record teaches each and every feature of the claim. In view of the foregoing and in contrast to the Office's assertions, the Applicants submit that the combination of Brune, Crawford, and Beigel fails to teach each and every feature of claim 16, and therefore fails to render claim 16 prima facie obvious under 35 U.S.C. 103. Thus, the Applicants kindly request the Office to withdraw the outstanding rejection of claim 16.

Claims 2 and 3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Herz in view of Brune. These rejections are traversed.

Because each of claims 2 and 3 incorporates the features of claim 1 from which it depends, each of claims 2 and 3 is patentable for at least the same reasons provided above with regard to claim 1.

Claims 4-7, 17, and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Herz in view of Brune, and in further view of Crawford. These rejections are traversed.

Because each of claims 4-7 incorporates the features of claim 1 from which it depends, each of claims 4-7 is patentable for at least the same reasons provided above with regard to claim 1. Also, because each of claims 17 and 20 incorporates the features of claim 16 from which it depends, each of claims 17 and 20 is patentable for at least the same reasons provided above with regard to claim 16.

Claims 12-15 and 18-19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Crawford, and further in view of Herz. These rejections are traversed.

Because each of claims 12-15 incorporates the features of claim 11 from which it depends, each of claims 12-15 is patentable for at least the same reasons provided above

with regard to claim 11. Also, because each of claims 18-19 incorporates the features of claim 16 from which it depends, each of claims 18-19 is patentable for at least the same reasons provided above with regard to claim 16.

The Applicants submit that all of the pending claims are in condition for allowance. Therefore, a Notice of Allowance is requested. If the Examiner has any questions concerning the present Response, the Examiner is requested to contact the undersigned at (408) 774-6914. If any additional fees are due in connection with filing this Response, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP269). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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